

SQUEEZE

RF DESIGN, ONCE RELEGATED TO A FEW SPECIALISTS AND ITS OWN CHIP SET, IS NOW INTEGRATED WITH DIGITAL AND ANALOG MODULES IN THE SAME IC. MOREOVER, THE CRITICAL DIMENSIONS INHERENT IN RF DESIGNS ADD TO ENGINEERING PRESSURES.

RF design is the design of a circuit that can transmit electromagnetic signals. RF stands for radio frequency, because in their infancy, RF circuits could emit radio signals only in the AM and FM bands. To call high-frequency design "RF design" today is to use a historical label. Figure 1 reveals that broadcasting applications have used frequencies higher than 300,000 MHz since the 1960s, with the introduction of UHF TV.

Since then, communication applications have increased in content, frequency, and bandwidth. Joe Civello, ADS platform manager at Agilent Technologies, notes that the chal-

lenges for analog/mixed-signal-IC designers are increasing at an unprecedented rate. Driven by the market demand for higher bandwidth and more end-product capability, designs are moving into higher frequency ranges and growing in complexity. Engineers are integrating RF circuitry with analog and digital nanometer circuitry. Gigabit data rates are causing digital circuits to behave like microwave circuits. Pervasive, complex wireless-communication standards—such as WiFi (Wireless Fidelity) 802.11a/b/g, Ultra-Wideband, and Bluetooth—require circuit designers to evaluate the impact of their designs on overall system performance.

Form factor, power, and cost drive the increasing integration of analog, RF, and digital design. Portable-device applications require that equipment be small and light, consume as little power as possible, and keep costs to a minimum. Integration directly impacts the manufacturing costs of the final electronic product, the size and weight of the product, and, most often, the amount of required power. For every component that designers remove from the bill of materials, a subsequent drop occurs in the overhead to maintain the supply chain for that component, a drop occurs in the manufacturing costs for the final product, and a reduction in the size of the product probably occurs.

Bill Krenik, research manager for wireless applications at Texas Instruments, says that RF design has always been difficult, because the lack of proper instrumentation complicates the analysis of high-frequency signals. Engineers have had to take indirect measurements and infer the characteristics of the circuit from what they could observe about its behavior. As engineers implement digital, analog, and RF circuitry on the same die, integration issues have further complicated the problem. Digital signals traveling via the substrate or radiating across the surface of the IC affect the noise sensitivity of the RF or analog portions. Many of these insidious effects combine, resulting in first silicon fraught with problems. Traditional debugging methods may no longer apply—meaning that you must correctly create the design, accurately modeling as many of the physical effects as possible before the design goes to fabrication. When the design methodology fails to accurately model the silicon, the design team often has no choice but to manufacture the device and observe its behavior. Taking this path is a high-stakes bet and one

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that most companies prefer to consider only as a last resort.

Analog and RF circuitry has traditionally existed on its own chip, making it much easier to isolate noise in the system and prevent coupling into the sensitive nodes of the circuit. When engineers integrate these sorts of design components onto a single die, they cannot ignore the noise problem. Without some form of accurate silicon-substrate modeling, they might not even know these problems exist until silicon comes back from the fab. Almost always, the development of this type of product requires a team of experts that specialize in various engineering disciplines. Individual designers rarely have both RF expertise and analog expertise; moreover, the RF experts and the analog experts use different development tools and may reside in different geographical locations, leading to increased difficulties during final chip integration.

Each unique design domain has its own methods and techniques for the development and testing of modules. The methods engineers use to design analog differ radically from the methods for digital, and, for that matter, analog differs significantly from RF. For instance, there is no equivalent of Boolean algebra to support synthesis in the analog and RF domains. And simulating a digital block in the frequency domain has no meaning. Because of these fundamental differences, a mismatch often exists between design methods that you must consider before the start of the design. Designers almost always perform digital design in the time domain and RF design in the frequency domain (for simulation speed). Integrating these two design styles on the chip can mean that simulation time of the entire chip is unrealistically long. The same situation is true for the test and verification phases of the design flow. The tests for digital differ from those for analog, and, again, the analog portion of the design differs from the RF portion. In spite of the problems, designers have developed and continue to develop products that integrate all three disciplines.

Doug Grant, director of business development in the RF and wireless group at Analog Devices, recounts a successful engineering development in spite of the tools' shortcomings. When Analog Devices decided to use the direct-conversion, or "zero-IF" architecture to reduce component count and cost in the Othel-

AT A GLANCE

- ▷ RF designers must often deduce the causes of a circuit's malfunction using indirect measurements of its behavior.
- ▷ RF-design issues are impacting digital and analog designs.
- ▷ Integration of RF circuitry on the same pc board or IC forces a new design methodology.
- ▷ EDA vendors are beginning to provide analysis tools that integrate time- and frequency-domain simulation.

lo family of RF transceivers, designers had to solve the architecture problems using a variety of techniques. Direct conversion, especially when you apply it to a time-division-multiplexed system such as GSM (global system for mobile communications), presents big problems with dc offset correction, because the system must compensate for the offset on each burst, and the offset varies from burst to burst. Most customers and competitors strongly advised against using direct conversion, citing other suppliers' previous failed attempts. The first problem was as much as possible minimizing the offset with careful design in the transmitter circuitry. The first step, which designers performed at the RF-system level, was a frequency plan that minimized self-mixing due to local-oscillator leakage. Careful design of the high-gain baseband amplifiers and filters was next; it required classical analog-design tools and simulation and resulted in good—but not good enough—performance.

Engineers added low-resolution DACs to provide a software-controllable dc offset adjustment to improve matters, but it still wasn't enough for all possible conditions. Further reduction in offset would have required more power and chip area, so the mixed-signal designers and the system designers had to find a common solution. The system designers advised that a few more decibels of dynamic range were necessary to absorb the residual offset. ADC designers responded with an improvement over previous designs that minimally increased power, using a combination of analog- and digital-design tools and simulations. The system team then worked with the physical-layer-software team to improve the algorithm for

channel compensation with an improved offset-correction routine that did not greatly increase processing power. The result of the team efforts was a robust direct-conversion transceiver.

RF DESIGN

Designers of RF circuits must deal with four types of issues during the planning and development of their products, states Dave Robertson, product-line director in the high-speed-converter group at Analog Devices. They must consider business issues, such as die size, yield, and time to market, and they must take into account the interoperability standards that will open the largest possible application market to the product. Engineers also must consider the frequency domain in which the product will operate. The target band can be either licensed or unlicensed, but, in either case, it will be under the regulatory authority of both national and international agencies. Finally, designers must deal with the product's physical layer, where they will need to solve a number of nonlinear problems.

At the system level, designers of wireless products must evaluate the overall function and performance of the system, including data throughput, channel interference, and power consumption. The results help system architects to define the design components and their requirements and specifications for use in circuit-level design. Circuit designers implement each component at the transistor level and, ideally, should be able to use the system-level specification as a test-bench to verify the component performance against the system requirements. At the physical-implementation level, designers produce a layout of each RF component and package each component in one or more devices, depending on the original product requirements. They must verify the layout, including device and interconnect parasitics, to ensure final performance and manufacturability. Design engineers integrating an RF device into a product must have a way to evaluate the system performance before the design reaches completion.

James Spoto, president and chief executive officer of AWR (Applied Wave Research), observes a challenge in that all these design domains or phases are isolated by disjointed EDA environments and databases and use tools and models that are not designed for gigahertz fre-

quencies. Poor correlation exists between the architectural models and the actual circuit performance. Architectural models ignore or poorly approximate many RF-circuit impairments, such as noise, distortion, and impedance mismatch.

Analog Office design suite from AWR aims to alleviate the problem. It focuses on total RF closure and offers a concurrent interconnect-driven and RF-aware design methodology in a unified design environment spanning the IC-design flow—from system- to circuit-level design and verification. It includes design entry and schematic capture, time- and frequency-domain simulation and analysis, physical layout with automated device-level placement and routing and integrated design-rule checker, 3-D full-field solver-based extraction that uses technology from OEA International (www.oea.com), and a comprehensive set of waveform-display and analysis capabilities supporting RF measurements.

Ansoft Corp supports RF design with Ansoft Designer, which provides data entry and visualization together with time, frequency, and mixed-mode simulation. For system-level simulation, in addition to its library of RF and DSP components, it supports compiled and interpretive C and C++ user-defined model cosimulation as well as The Mathworks' Matlab cosimulation. Circuit-simulation solutions include analysis for nonlinear-noise, transient, digital-modulation, nonlinear-stability, and load-and-source pull. It also provides design synthesis for filters and transmission lines. The product includes a layout-and-manufacturing module as well as a 3-D planar electromagnetic-simulation engine.

The Genesys suite of products from Eagleware contains schematic entry, a number of simulation engines, synthesis capabilities for a number of analog circuits, and production and customization capabilities. The simulation engines support linear-circuit simulation, spectral domain-system simulation; harmonic-balance nonlinear simulation; and multilevel, planar-3-D-electromagnetic simulation. It provides synthesis for transmission lines, op-amp filters, LC and direct LC/dis-

tributed filters, phase-lock loops, oscillators, microwave distributed filters, and circuits to perform delay equalization and impedance matching.

Neoliner provides RF designers with NeoCircuit-RF. The tool offers design entry, simulation, and synthesis for a range of RF components. It uses Cadence's SpecTre RF and Agilent's ADS simulators to interactively or automatically size, bias, and verify custom RF circuits. Engineers can take measurements using built-in capabilities, or they can add their own proprietary measurements through an open API (application-programming interface). NeoCircuit-RF can distribute the synthesis task over many machines using LSF (www.platform.com) or Grid Engine (www.gridengine.sunsource.net) to properly manage the available execution license among the team members.

A number of RF design platforms integrate Agilent Technologies' ADS (Advanced Design System). It offers several simulation engines, including ac, dc, S-parameter, and harmonic-balance simulation, as well as circuit-envelope simulation and transient and convergence simulation. It is not surprising that, according to Dataquest, Agilent Technologies is the market leader for RF design.

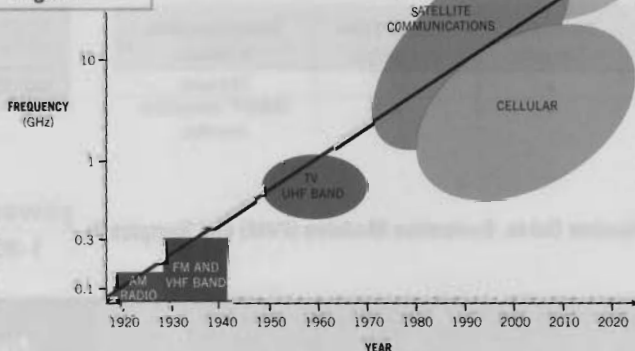
Depending on the size of a design, RF effects can become noticeable at frequencies as low as a few megahertz. Even clocks operating as low as a few hundred megahertz have frequency components well into the gigahertz range. These high-frequency harmonics of fundamental clock rate can easily radiate off the board or the chip and cause noise and interfer-

ence problems elsewhere in the design. Analog and digital designers are now seeing the undesirable consequences of "high frequencies" in their designs in the form of signal contamination, crosstalk, substrate coupling, and parasitic effects. The industry uses the term "signal integrity" to describe unwanted RF effects in digital design. **Reference 1** describes EDA tools that will help you avoid some of these problems. Parasitic-extraction tools and time-domain simulators replace ideal wires with models that describe their behavior when high frequencies are present. Although these tools are better than no modeling of parasitic effects, they are only first-order approximations of the full RF nature of traces. More detailed and accurate electromagnetic and convolution modeling software helps solve the most important and sensitive parts of the design but takes more time to simulate and is practical only over small areas of a layout or package design.

Engineers have traditionally designed RF circuits on separate, isolated modules. The drive to reduce form factors for consumer electronics, such as mobile phones and PDAs, has led to the design of pc boards that integrate RF circuits. The design challenges depend on the operating frequency. At lower frequencies, you can place discrete RF elements on the board and connect them with impedance-controlled traces and vias. At designs requiring higher frequencies, designers must use transmission lines and device models for all physical elements by using parametric shapes with precalculated scattering, or S-, parameter models. The drive

to reduce space has even led to the interactive modification of these predefined parametric shapes. To verify the circuits, you must first use a 3-D electromagnetic field solver to create models of the transmission lines. You must then use a circuit simulator for functional verification. The integration of high-speed devices capable of gigabit data speeds has raised the bar for high-speed design and simulation and requires more accurate models to describe the communi-

Figure 1



The frequency spectrum used in modern applications is much wider than the classical RF band.

cation architecture within these devices.

Digital designers are used to packaging logical functions into predefined components and then connecting them on a pc board. RF circuits at high frequencies employ few predefined components; the interconnecting transmission lines, including traces, vias, and conductive shapes, create the functional circuit. This method requires a strong understanding of RF-circuit behavior, and it relies heavily on electromagnetic and circuit simulators. RF circuits are also noisy and sensitive, requiring physical isolation.

Both high-speed and RF design involve accurate modeling of interconnecting transmission lines. High-speed circuits employ complex, discrete digital components. RF circuits include the components within the metallization layers, eliminating discrete components. In RF design, the interconnecting traces provide the modeling complexity and require the use of 3-D electromagnetic field solvers. In RF-analog narrowband design, the transmission-element shapes provide passive elements for the circuit, such as capacitors, inductors, and shorts. They work over only a narrow range of frequencies in which the intended signal is expected to operate. At other frequencies, these shapes would have undesirable characteristics. So, the pc-board copper configuration of an "RF-analog" design targets a relatively narrow-frequency-band signal. Although both semiconductor and EDA vendors are working to develop accurate models of RF devices that they will be able to efficiently simulate, most designers still rely on design guidelines and reference designs from RFIC vendors.

Engineers use high-speed serial I/O because it delivers higher performance, lower costs, and simpler designs. The Xi-

linx RocketPHY transceiver can operate at 10 Gbps, allowing designers to use serial connections that operate faster than traditional parallel-bus architectures. Designing with multigigabit serial-I/O technology requires greater attention to issues that affect signal integrity, such as attenuation, noise, and reflections. Engineers must therefore analyze the design with techniques that normally only RF designers use, because the exact characteristics of distributed parasitics are critical to the overall behavior of the system. Engineers often use S-parameters to characterize the parasitics associated with transmission lines, packages, and connectors. The HSpice simulator from Synopsys provides a rich set of analysis features, golden models, and native S-parameter model support. Xilinx designers used HSpice to characterize the RocketPHY transceiver during its development.

Mentor has some design and verification tools for pc-board RF design in addition to leveraged alliances with key RF-design vendors, such as Agilent Technologies. Mentor has modified its core-design-definition and -layout products, Board Architect and Board Station, to understand RF elements. You can simulate mixed-signal circuits with System Vision, combining the power of the ModelSim and ADMS simulation engines. Mentor has updated its ICX and HyperLynx simulators to handle more accurate transmission-line models, such as lossy transmission lines and frequency-dependent vias.

PCB Design Expert from Cadence allows engineers to import design modules of RF subcircuits, interface with signal-analysis tools, and define and constrain critical high-speed signals at all stages of the design process.

The major challenge for designers of digital, analog, and RF ICs is finding a suitable simulation environment in which they can evaluate possible solutions and verify the chosen approach. Historically, designers of high-frequency systems used frequency-domain-simulation technology to develop RF and microwave components, and analog/mixed-signal-system designers used time-domain-simulation technology to develop large-scale ICs and worked separately on their own piece of the design. Engineers of analog/mixed-signal systems design many of today's RF/mixed-signal ICs and use time-domain-simulation technology (Spice) to look for voltage gain, ac sweeps of voltage gain and impedance, noise voltage, and so on. But EDA vendors have developed most of the technology targeting high-frequency applications using frequency-domain-simulation technology. RF engineers, concerned with frequency-domain data, are comfortable designing circuit blocks using frequency-domain-simulation tools.

With the emergence of highly integrated, large-scale RF/mixed-signal ICs, designers of high-frequency and analog/mixed-signal systems now must share silicon. At the same time, design teams are implementing complete systems by combining high-frequency, analog, and digital components, using multiple semiconductor technologies, onto highly integrated modules.

This situation is leading to a convergence of design methodologies and the emergence of the unified RF/-mixed-signal-design group. From the perspective of designers of high-frequency systems, the size and complexity of the design are increasing, leading to an increased need for time-domain-simulation technology to

complement familiar frequency-domain-simulation technology. From the perspective of analog/mixed signal designers, the data rates and signal frequencies are increasing, leading to an increased need for frequency-domain-simulation technology to complement familiar time-domain-simulation technology.

One way to handle the problem of simulating a design that requires both time- and frequency-domain analysis is to abstract all descriptions into behavioral models so that you reduce the

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computation burden for the simulator and keep the CPU time reasonable. With these methods, the RF and analog blocks and signals are either linearized or simplified to "baseband" models, so that you maximize simulation speed. Matlab is a popular tool for architectural exploration of mixed-mode designs. It and other tools using this approach employ proprietary description languages, which are often close to C or C++ in their structure and capabilities. They use data-flow algorithms and usually achieve faster simulation than do HDL simulators. Fast, all-behavioral simulation is certainly desirable and useful in some circumstances, but many senior system architects complain that these simulations teach them little that they don't already know.

A fundamental discontinuity exists between architectural design and implementation. You cannot proceed to implementation with the design description in the format that architectural exploration uses. When moving toward real implementation, you must describe the RF and analog blocks in much greater detail—ultimately down to the transistor level—using different implementation languages.

The Spice family of circuit simulators is still the most popular for analog design. But to achieve the needed accuracy of results, Spice simulations require long executions. In the last couple of years, EDA vendors have offered "fast-Spice" simulators that use table look-up models, timing algorithms, or both instead of the traditional Spice algorithm. These tools significantly decrease simulation times in the analog- and mixed-signal world, most successfully when you need to simulate large digital blocks at the transistor level. However, for applications including an RF front end, either the accuracy is insufficient or the accuracy settings must be so tight that the increase in execution speed is negligible. A typical RFIC contains an RF front end, analog-processing functions, and a large quota of digital logic and DSP functions. The analog and DSP blocks are usually tightly linked and best simulated with mixed-signal simulators. You can consider RF signals as special analog signals and use a mixed-signal simulator to analyze your design. This approach seems to provide all the required degrees of flexibility. To gain speed, you can abstract noncritical blocks as behavioral models, using either the IEEE-standard VHDL AMS or the

more vendor-dependent Verilog AMS. You can describe critical blocks in Spice to gain accuracy. However, mixed-signal simulators use time-domain algorithms, just like Spice-style simulators, for the analog portions.

Time-domain algorithms create insurmountable performance problems for RFIC simulation, because extensive verification of an RFIC requires support of

A FUNDAMENTAL DISCONTINUITY EXISTS BETWEEN ARCHITECTURAL DESIGN AND IMPLEMENTATION.

digitally modulated signals. The system must impress all these complex signals onto RF carriers of 1 to 10 GHz, depending on the wireless standard employed. But the modulation information is usually at much lower frequencies, typically a few hundred kilohertz or megahertz. The symbol period is typically about 1 μ sec. Engineers must analyze thousands of symbols to verify such systems. The simulator must execute a huge number of RF-carrier cycles, with time steps of tenths of picoseconds. Such a simulation would take weeks to execute and generate gigabytes of output files. Therefore, time-domain simulation is inappropriate for the efficient analysis of digitally modulated signals.

Mentor has developed the ADMS RF mixed-signal/mixed-domain simulator. It is "language-neutral" and uses only industry-standard IC-design languages. It supports Spice, Verilog, VHDL, Verilog AMS, and VHDL AMS. You can even link C modules from the VHDL code. Engineers can thus describe each block using the design language most appropriate for the desired level of abstraction. ADMS RF exploits the special nature of digitally modulated signals to improve simulation performance.

Agilent Technologies and Cadence formed the RF/MS IC Alliance to combine the RF and IC design environments and to address the increasing challenges of RF/mixed-signal-IC design. The RFDE (RF Design Environment) gives designers access to Agilent's frequency-domain circuit-simulation technology and Cadence's time-domain circuit-simulation technology, all within the Cadence IC-design flow. With the latest release of

RFDE, Wireless IC, designers can directly verify their Cadence-based RF-circuit schematics with various baseband architectures. They can develop testbenches early in the development cycle and export them from Agilent's Advanced Design System into RFDE. RFIC designers can then access the testbenches from within the Cadence-analog and mixed-signal design flow, to verify their circuit designs before taping out to silicon. In addition, several preconfigured wireless testbenches are available as RFDE options. RFDE wireless testbenches use Agilent's simulation technologies, such as Circuit Envelope, Agilent Ptolemy, and AMI (Automatic Verification Modeling).

The Agilent Connection Manager works with RFDE wireless testbenches to download data from RFDE to test instrumentation so that designers can perform system verification earlier in the development cycle. Users can also generate accurate electromagnetic-based models of passive on-chip components and interconnects using Agilent Momentum—a 2.5-D method-of-moments-based simulation technology. You can directly simulate the electromagnetic-based models in the Cadence circuit schematic without the usual conversion to approximate lumped-element models, obtaining greater accuracy for wireless and high-speed wire-line applications. Momentum electromagnetic modeling and verification is also a synergistic tool with existing resistor-capacitor-extraction tools. It helps add needed modeling accuracy to critical design nets, in which failure can damage an entire process run.

CONNECTIVITY ISSUES IN RFIC DESIGN

ARF-circuit performance is the direct result of the physical implementation that the combination of designers and EDA tools achieves. Many of the issues that designers must deal with in RF design are also gaining importance in digital and mixed-signal designs as features dimensions continue to shrink. Modeling of parasitics and interconnections further complicates simulation problems. Yet, accurate RF device models must include parasitic element networks. Also, accurate representation of the interconnections is necessary because of the high frequency of operation. At several gigahertz, once-negligible parasitic elements can cause chip failure. The on-chip interconnections, the bonding wires, and

the off-chip microstrip-type interconnections always or sometimes require attention. In addition, modeling of the chip substrate is often necessary to capture the noise that the digital signals induce. Designers model both on-chip interconnection and substrates with large parasitic networks, which may challenge the capacity of the simulators. Most foundries today delivering RF processes provide accurate simulation models of the devices as parts of a process-design kit.

The models are organized as hierarchical subcircuits, each describing the circuitry of a device. Each model includes the basic primitive element and a nontrivial network of passive elements and internal nodes to model the additional physical detail that accurate simulation at RF frequencies needs. For example, the passive elements may model drain/source-access networks, junction diodes, substrate networks, gate-current networks, and parasitics due to the layout of the device.

The basic model of the primitive component either ignores or poorly represents these effects. Some of the compo-

nents in the parasitic network, such as spiral inductors, may even directly depend on operating frequency. These frequency-dependent components are particularly costly to simulate in a conventional transient simulator. They are much easier to handle in the frequency domain. Thus, for each RF device in a schematic, the simulator must handle four or more additional internal nodes and 10 or more passive elements. Even before taking into account interconnections, the complexity of the actual simulation data is one order of magnitude higher than the schematic-level data, each device counting for much more than a simple primitive.

For accurate simulation, designers must extract interconnection between the critical RF blocks from the layout and simulate them along with the active devices. RF designers rarely have the luxury of designing blocks with input and output impedances so that they can easily interconnect the blocks. They can rarely design RF blocks without detailed information about the interconnection

drive and the load lines to which it will connect, once they integrate the blocks into the final circuit. This limitation is another reason that behavioral modeling is an incomplete answer to the problem.

Creating a behavioral model of the input/output stages that capture the interaction detail with the interconnection is usually too complicated. Devices such as preamplifiers or power amplifiers, in which large current swings can cause significant voltage drops in seemingly negligible parasitic resistors, need accurate interconnection modeling. Designers can configure the layout-extraction tools on the market to generate either R (resistance), RC (resistance-capacitance), RCC (coupling capacitances), or even RLCK (inductance and inductance-coupling-coefficients) networks. The smaller geometries and higher frequencies make it challenging to perform the physical modeling of IC wires. Usually, the extraction tool produces a Spicelike netlist that any simulator that accepts the Spice syntax can read. However, the extracted netlist can sometimes be tens of millions



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of elements, particularly when it includes RCC or RLCK. The extraction tool and the simulator must provide corrective measures when the size of the parasitic network too severely slows simulation. You should be able to reduce the size of the network by altering extraction parameters. You should also be able to reduce the network to a smaller equivalent network with extractor or simulator controls. In addition, you can enhance simulation accuracy by removing negligibly small resistors from the network.

The substrate-modeling problem is somewhat similar to the interconnection problem. Overdesigning with huge guard rings in an attempt to shield the sensitive analog and RF blocks from digital noise is often an unacceptable use of silicon area. To model the substrate, designers use either Spice-equivalent networks of their own or commercial tools to extract an equivalent network from the layout information. These networks are usually reduced RC networks, but they can still substantially burden the simulator.

Accurately modeling the physical ef-

fects of bonding wires may be critical at the frequencies of interest in a system-on-chip that contains RF circuitry. A variation in impedance of a fraction of a nanohenry due to a bond wire may well destabilize a stable design. Designers generally use one of two analysis methods, depending on the criticality. Most designers use Spice-equivalent networks, and others apply electromagnetic simulation to the actual physical structures to obtain an S-parameter description. They can then simulate the S-parameter block together with the active devices.

These access networks are fairly linear, and using S-parameters is efficient. However, the cost of electromagnetic simulation can be high, particularly if you need a large bandwidth. You can simulate S-parameters either in the time or the frequency domain. Again, the frequency domain is an obvious better choice in simulation speed. Whatever the modeling method (Spice-equivalent or electromagnetic), the re-

sulting network remains relatively small. (The number of pads does not grow exponentially with each generation.) Bonding wires may be tricky to model, but they do not create an excessive simulation burden. Some applications require the simulation of off-chip interconnections together with the IC. For example, designers may have to consider I/O-matching networks an integral part of the system. In such cases, you usually model off-chip interconnections as microstrip structures, best defined and thus simulated in the frequency domain.

Mentor's ADMS RF tool allows designers to apply all of these analysis techniques at the physical-design level. RFDE, the result of the Agilent/Cadence collaboration, also helps designers perform physical analysis of their designs. □

REFERENCE

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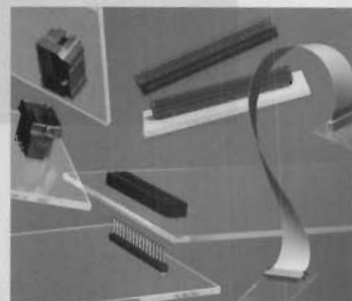
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